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ABSTRACT OF THE DISCLOSURE

An interface connects data processing components and data  
5       memories that support data transfer at different data rates.  
The interface handles complex timing and asynchronous delays  
associated with these different rates of data transfer. The  
interface may be used to connect data processing components  
that operate at 133 MHz with DDR SDRAM devices that operate at  
10      200 MHz to 266 MHz data rates.

SDB/dlf

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